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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,427	07/03/2003	Jarrod Eliason	RAM 493 DIV	5188

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EXAMINER	
LAM, TUAN THIEU	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,427	ELIASON, JARROD	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39,42,43,45,49-52,54,56,58,60 and 81* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39,42,43,45,49-52,54,56,58,60 and 81* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the amendment filed 8/31/2004. Claims 1-39, 42-43, 45, 49-52, 54, 56, 58, 60 and 81 are pending.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-39, 42, 43, 45, 49-52, 54, 56, 58, 60 and 81 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 81, the recitation of "a ferroelectric capacitor circuit .. coupled between the internal node of the first logic gate and the internal node of the second logic gate" is indefinite because it is misdescriptive of the present invention. As shown in figure 4, the ferroelectric capacitor circuit (z0, z1, z10 and z11) coupled to ground and selective coupled to the Q output and complementary Q output via the switches controlled by WL and WLB signals. The ferroelectric capacitor circuit is not coupled between the internal node of the first logic gate and the internal node of the second logic gate as recited. Applicant is required to particularly point out the internal nodes of the first and second logic gates and explain as to how the ferroelectric capacitor circuit coupled to the internal nodes of the first and second logic gates as recited. Clarification and correction are required.

In claims 6 and 7, the recitation of "internal circuit node of the first NAND gate" (lines 3-4), "internal circuit node of the second NAND gate" (lines 5-6), "internal circuit nodes of the first and second NAND gates" (lines 7-8) is indefinite because it is misdescriptive. As shown in

figure 4, "internal circuit node of the first NAND gate" (lines 3-4) is supposed to be --Q output--, "internal circuit node of the second NAND gate" (lines 5-6) is supposed to --complementary Q output--, "internal circuit nodes of the first and second NAND gates" (lines 7-8) is supposed to be --Q and complementary Q outputs--. Correction is required.

In claim 8, the recitation of "means for selectively coupling the ferroelectric capacitor circuit" is indefinite because it is incomplete. It is unclear as to the where the ferroelectric capacitor circuit is coupled to. As shown in figure 4, the ferroelectric capacitor circuit (z0, z1, z10 and z11) is selectively coupled to the gates of the transistors N1PA and N1NA via a first switch and to the gate of transistors N2PA and N2NA via an another switch. Correction is required.

In claim 9, the recitation of "a pass gate circuit for selectively coupling the ferroelectric capacitor circuit" is indefinite because it is incomplete. It is unclear as to the where the ferroelectric capacitor circuit is coupled to. As shown in figure 4, the ferroelectric capacitor circuit (z0, z1, z10 and z11) is selectively coupled to the gates of the transistors N1PA and N1NA via a first switch and to the gate of transistors N2PA and N2NA via an another switch. Correction is required.

Claims 1-5, 10-39, 42-43, 45, 49-52, 54, 56, 58 and 60 are indefinite because of the technical deficiencies of claim 81.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 81, 1, 10, 11, 12, 14, 23, 24 remain rejected under 35 U.S.C. 102(b) as being anticipated by W0 01/15323 A1 cited by the applicant's PTOL-1449. Figure 4 of W0 01/15323 A1 show an RS flip flop comprising a set input (SETB), a reset input (RESETB), a Q output (Q), complementary Q (QB), a first NAND gate (24) having an internal node, a second NAND gate (25) having an internal node, a ferroelectric capacitor circuit comprising at least one ferroelectric load capacitor (16, 17) and at least one ferroelectric storage capacitor (14, 15) coupled between the internal node of the first logic gate and the internal node of the second logic (as discussed in the 112, second paragraph rejection, the ferroelectric capacitor circuit is coupled to the output and complementary output, therefore, the limitations of "coupled between the internal node of the first logic gate and the internal node of the second logic" is interpreted as "coupled between the output and complementary output of the first and second logic gates") as called for in claims 81 and 1.

Regarding claims 10 and 23, precharge circuit is seen as transistors 18, 19.

Regarding claims 11 and 24, equalizing circuit are seen as capacitors 16, 17.

Regarding claims 12 and 25, gate control circuit is seen as transistors 32 and 33 of figure 5.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-5 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over W0 01/15323A1 in view of applicant's cited prior art figures 2 and 14. Figure 4 of W0 01/15323 A1 show an RS flip flop comprising a set input (SETB), a reset input (RESETB), a Q output (Q), complementary Q (QB), a first NAND gate (24) having an internal node, a second NAND gate (25) having an internal node, a ferroelectric capacitor circuit comprising at least one ferroelectric load capacitor (16, 17) and at least one ferroelectric storage capacitor (14, 15) coupled between the internal node of the first logic gate and the internal node of the second logic (as discussed in the 112, second paragraph rejection, the ferroelectric capacitor circuit is coupled to the output and complementary output, therefore, the limitations of "coupled between the internal node of the first logic gate and the internal node of the second logic" is interpreted as "coupled between the output and complementary output of the first and second logic gates"). The W0 01/15323A1 does not show the detailed structure of the first and second logic gates. Applicant's admitted prior art figure 2 has only eight transistors and low power consumption. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to use the circuit arrangement of applicant's admitted prior art figure 2 of the cross coupled NAND gates of W0 01/15323A1 for the purpose of low power consumption.

7. Claims 27-31 and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leuschner (USP 4,002,933) in view of W0 01/15323A1. Figure 1 of Leuschner shows JK flip flop comprising a RS flip flop (G4, G5), a J input (J), a K input (K), a clock signal (CK), first NAND (G3), a second NAND gate (G2). Leuschner shows a standard RS flip flop instead of a ferroelectric RS flip flop as called for in claim 27. Figure 4 of W0 01/15323 A1 show a ferroelectric RS flip flop comprising a set input (SETB), a reset input (RESETB), a Q output (Q),

complementary Q (QB), a first NAND gate (24), a second NAND gate (25), a ferroelectric capacitor circuit (14, 15). Ferroelectric RS flip flop provides a higher operational speed than the standard RS flip flop. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to replace Leuschner's standard RS flip flop (G4, G5) with W0 01/15323A1's ferroelectric RS flip flop for the purpose of increasing operational speed.

Regarding claims 28 and 29, the NAND and NOR gates are seen in figure s 3 and 4 of W0 01/15323 A1.

Regarding claims 30 and 31, the controlled power supplies are seen as the PCS and NCS of figure 5 of W0 01/15323 A1.

Regarding claim 35, precharge circuit is seen as transistors 18, 19 of W0 01/15323 A1.

Regarding claim 36, equalizing circuit are seen as capacitors 16, 17 W0 01/15323 A1.

Regarding claim 37, gate control circuit is seen as transistors 32 and 33 of figure 5 of W0 01/15323 A1.

Response to Arguments

8. Applicant's arguments filed 8/31/2004 have been fully considered but they are not persuasive. In the construction of claim 81 corresponding to figure 4 of the present invention, applicant states that the switch is part of the logic gate, one end of which forms the internal circuit node of the logic gate that is coupled to the ferroelectric capacitor circuit is not persuasive. Applicant has not particularly pointed out what are the internal nodes and as to how the ferroelectric capacitor circuit coupled between the internal node of the first logic gate and the

internal node of the second logic gate. Therefore, claim 81 remains indefinite under 35USC 112, second paragraph.

9. Regarding the rejection of claims 81, 1, 10, 11, 12, 14, 23 and 24 under 35USC 012(b), applicant argues that the ferroelectric capacitor circuit (14-17) of W0 01/15323 is not ferroelectric capacitor circuit is not persuasive. The elements 14-17 are clearly shown as ferroelectric storage capacitor and load capacitors. Therefore, the rejection is deemed to be proper.

10. Applicant also argues that the ferroelectric capacitor circuit of W0 01/15323 is not coupled between the internal nodes of the first and second logic gates is not persuasive. As discussed in the 112, second paragraph rejection, the ferroelectric capacitor circuit, as seen in figure 4, is coupled to the output and complementary output, therefore, the limitations of "coupled between the internal node of the first logic gate and the internal node of the second logic" is interpreted as "coupled between the output and complementary output of the first and second logic gates". Therefore, the limitations of claim 81 are fully met.

11. The independent claim 81 remains rejected, thus, the dependent claims 2-5, 15-18, 27-31 and 35-37 also remain rejected.

Allowable Subject Matter

12. Claims 6-9, 13, 19-22, 26, 32-34, 38-39, 42-43, 45, 49-52, 54, 56, 58 and 60 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In this regard, applicant's cited prior art in the PTOL-1449 has been carefully considered.

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam
Primary Examiner
Art Unit 2816

10/4/2004